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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,150	12/03/2003	Jin-Yuan Lee	JCLA8534-D	6802

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EXAMINER	
THAI, LUAN C	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 11/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/728,150	LEE ET AL.	
	Examiner	Art Unit	
	Luan Thai	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,6-9,13-17,25-29,176,177,180,186-189,193-196,200,202 and 203* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6-9,13-17,25-29,176,177,180,186-189,193-196,200,202 and 203* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/055,499.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Embodiment V of Figs. 9-11 with claims 1, 6-9, 13-17, 25-29, 176, 177, 180, 186-189, 193-196, 200, and 202-203 being read on the elected Embodiment, dated 8/17/04, is acknowledged. Claims 2-5, 10-12, 18-24, 30-175, 178-179, 181-185, 190-192, 197-199, and 201 are canceled. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a).

Priority

2. This application appears to be a division of Application No. 10/055,499, filed 01/22/02.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 6-9, and 13-17, are rejected under 35 U.S.C. 102(b) as being anticipated by Saito et al (5,049,980 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1, 6-9, and 13-17, Saito et al (see specifically figures 1-5) disclose a chip package structure comprising: an organic (e.g., thermosetting plastic) substrate (1) with a surface; a plurality of dies (2), wherein each die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads (3) located on the active surface, whereas the backside of each die is adhered to the surface of the organic substrate (1); a thin-film circuit layer comprising: a first dielectric layer (4) of polyimide having a plurality of first thru-holes (5) (see figure 2) and located on top of the surface of the substrate (1) and the active surface of the dies (2), a first patterned wiring layer (7) located on top of the first dielectric layer (4), wherein a conductive material fills the thru-holes (5) to form a plurality of first vias (6), wherein the first patterned wiring layer (7) is electrically connected to the metal pads (3) of the dies (2) through the first dielectric layer (4) by the vias (6) and extends to a region outside of an area above the active surfaces of the dies. Saito et al. further disclose a second dielectric layer (9) on top the first dielectric layer and the first patterned wiring layer; a second patterned wiring layer (11) on top the second dielectric layer (9), wherein the second patterned wiring layer is electrically connected to the first patterned wiring layer (7) at bonding pads via conductive vias or bonding points (10) formed through the second dielectric layer (9), and wherein the patterned wiring layers (7/11) and the vias 6/10) form the external circuitry.

5. Claims 1, 6-9, 13-17, and 27-29, are rejected under 35 U.S.C. 102(e) as being anticipated by Wachtler et al (6,274,391 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1, 6-9, 13-17, and 27-29, Wachtler et al (see specifically figures 8-22) disclose a chip package structure comprising: an organic substrate (12) made of molded plastic; a plurality of dies (16)/(52) (Col. 11, lines 41-67 and Col. 12, lines 1-9), which are performed same functions or different functions (Col. 7, lines 58+), wherein each die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads (Col. 8, lines 63-67) located on the active surface, whereas the backside of each die is adhered to the surface of the organic substrate by a adhesive (Col. 8, lines 53+); a first dielectric layer (26/24) of polyimide on top of the surface of the substrate (12) and over the active surface of the dies (Col. 8, lines 59+); a plurality of first thru-holes (28) formed through the first dielectric layer (26/24) (see figures 11-12); a first patterned wiring layer (34/36) on top of the first dielectric layer (24/26), wherein the first patterned wiring layer fills the first thru-holes (28) and electrically connected to the metal pads of the dies (16). Wachtler et al further disclose a second dielectric layer (36/38) on top of the first patterned lines (32/34); a plurality of second thru-holes (40) formed through the second dielectric layer (see figures 16-17); a second patterned lines (42) on top the second dielectric layer (36/38), wherein the second patterned lines extend through the second dielectric layer, are electrically connected to the first patterned lines, and has a plurality of second bonding pads (44); a patterned passivation layer (46) on top of the

second patterned lines and exposing the second bonding pads (44); solder balls (22), which are considered as bonding points, electrically connected to the bonding pads (44).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 6-9, 13-17, 25-29, 176-177, 180, 186-189, 193-196, 200 and 102-203, are rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al (6,396,148 of record) in view of Marcinkiewicz (6,025,995 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1, 6-9, 13-17, 25-29, 176, 177, 180, 186-189, 193-196, 200, and 202-203, Eichelberger et al (see specifically figures 1-7) disclose a chip package structure comprising: a substrate (101) with a surface; a plurality of dies (102), wherein each die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads (107) located on the active surface, whereas the backside of each die is adhered to the surface of the substrate by a adhesive (103); a filling layer (104) of polymer or epoxy over the substrate (101) and surrounding the peripheral of the dies (102), wherein a top surface of the filling layer (104) being planar to the active surface of the dies (104) (see figures 3A and 4A). Eichelberger et al. further disclose a first dielectric layer (106) of polyimide over the top surface of the substrate (101) and over the

active surface of the dies (102), a plurality of first thru-holes (122) formed through the first dielectric layer (106) (see figures 3D and 4B); a first patterned wiring layer (108), wherein the first patterned wiring layer (108) is electrically connected to the metal pads (107) of the dies (102) through the first dielectric layer (106), wherein the first patterned layer (108) has a plurality of first bonding pads electrically connected to solder balls (110), which are considered as bonding points. Eichelberger et al further disclose: a patterned passivation layer (109/232) on top of the first dielectric patterned lines (108/206) and exposing the first bonding pads on the first patterned wiring layer (108) for solder balls (110) electrically connected to, as disclosed in figure 1. Eichelberger et al. further disclose that the similar dielectric layer and patterned wiring layer as described above can be repeatedly formed until all required patterned lines and dielectric layer have been completed (Col. 8, lines 53+). (Noted that figures 6C-7C also disclose passivation layer "232" is formed on top of the first dielectric patterned wiring layer "206" and exposing the first bonding pads on the first patterned wiring layer "209" for solder balls "234" electrically connected to. Eichelberger et al., however, do not explicitly teach the substrate comprising organic.

Marcinkewicz while related to a similar semiconductor structure design teaches the substrate (14) in the integrated circuit module (10) could be made by different kinds materials such as: plastic, silicon, etc., (Col. 3, lines 58+), which are considered as known materials for forming a substrate in semiconductor art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use plastic or silicon (e.g., organic material), to form the substrate in Eichelberger et al.'s chip package, since

such organic materials are well known in the art for making a substrate, as taught by Marcinkewicz, and since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 6:45 AM - 4:15 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Luan Thai
Primary Examiner
Art Unit 2829
November 3, 2004